

CLAIMS

What is claimed is:

- 1 1. An integrated circuit comprising:
2 an amplifier formed on a semiconductor die, the amplifier having an
3 output port with an output impedance; and
4 a bondwire electrically connecting the output port to an external
5 conductor;
6 wherein the bondwire has a specified self-inductance and is operable to
7 match the output impedance to a desired load impedance.
- 1 2. The integrated circuit of claim 1 wherein:
2 the amplifier is a radio frequency power amplifier.
- 1 3. The integrated circuit of claim 1 wherein:
2 the semiconductor die is a metal-oxide semiconductor die.
- 1 4. The integrated circuit of claim 1 wherein:
2 the semiconductor die is a gallium arsenide semiconductor die.
- 1 5. The integrated circuit of claim 1 wherein:
2 the semiconductor die is a bipolar semiconductor die.
- 1 6. A method for impedance matching comprising:

2 forming an amplifier on a semiconductor die, the amplifier having an
3 output port with an output impedance; and
4 connecting an electrically conducting bondwire between the output port
5 and an external conductor;
6 wherein:
7 the bondwire has a specified self-inductance and is operable to
8 match the output impedance to a desired load impedance.

1 7. The method of claim 6 wherein:

2 the amplifier is a radio frequency power amplifier.

1 8. An integrated circuit comprising:

2 an amplifier formed on a semiconductor die, the amplifier having an
3 output port with an output impedance;

4 a bondwire having a specified self-inductance and electrically connecting
5 the output port to an external conductor; and

6 a capacitor having a specified capacitance formed on the semiconductor
7 die and electrically connected between the output port and a ground, wherein:

8 the bondwire and the capacitor are operable to match the output
9 impedance to a desired load impedance.

1 9. The integrated circuit of claim 8 wherein:

2 the amplifier is a radio frequency power amplifier.

1 10. The integrated circuit of claim 8 wherein:

2 the bondwire, the capacitor and the desired load impedance are jointly
3 operable to resonate at a normal operating frequency of the integrated circuit.

1 11. The integrated circuit of claim 8 wherein:

2 the semiconductor die is a metal-oxide semiconductor die.

1 12. The integrated circuit of claim 8 wherein:

2 the semiconductor die is a gallium arsenide semiconductor die.

1 13. The integrated circuit of claim 8 wherein:

2 the semiconductor die is a bipolar semiconductor die.

1 14. A method for impedance matching comprising:

2 forming an amplifier on a semiconductor die, the amplifier having an
3 output port with an output impedance;

4 connecting an electrically conducting bondwire having a specified self-
5 inductance between the output port and an external conductor;

6 forming a capacitor having a specified capacitance on the semiconductor
7 die and electrically connected between the output port and a circuit ground,
8 wherein:

9 the bondwire and the capacitor are jointly operable to match the output
10 impedance to a desired load impedance.

1 15. An integrated circuit comprising:

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2 an amplifier formed on a semiconductor die, the amplifier having an
3 output port with an output impedance;

4 a first bondwire having a first specified self-inductance, and electrically
5 connecting the output port to a first external conductor;

6 a second bondwire having a second specified self-inductance, and
7 electrically connecting the first external conductor to a node on the die;

8 a first capacitor having a first capacitance formed on the semiconductor
9 die and electrically connected between the node and a ground;

10 a second capacitor having a second capacitance embodied on the
11 semiconductor die and electrically connected between the node and a third
12 bondwire, the third bondwire having a third specified self-inductance and
13 electrically connecting the second capacitor to a second external conductor

14 wherein:

15 the first, second and third bondwires and the first and second
16 capacitors are operable to match the output impedance to a desired load
17 impedance.

1 16. The integrated circuit of claim 15 wherein:

2 the amplifier is a radio frequency power amplifier.

1 17. The integrated circuit of claim 15 wherein:

2 the first capacitor is connected to ground via a further bondwire.

1 18. The integrated circuit of claim 15 wherein:

2 the further bondwire connects to a thermal pad formed within the
3 integrated circuit.

- 1 19. An integrated circuit comprising:
2 a semiconductor die;
3 a first bondwire having a first self-inductance electrically connected to the
4 die and to an external conductor;
5 a second bondwire having a second self-inductance electrically connected
6 to the die and to the external conductor, wherein:
7 the first and second bondwires are operable to act as an inductor to form at
8 least a part of a circuit block comprised within the integrated circuit.
- 1 20. The integrated circuit of claim 19 wherein:
2 the circuit block is an analog circuit.
- 1 21. The integrated circuit of claim 19 wherein:
2 the circuit block is a radio frequency circuit.
- 1 22. The integrated circuit of claim 19 wherein:
2 the circuit block is selected from a list consisting of:
3 an intra-stage match, an input stage match, a tuned circuit, an
4 oscillator, a filter, and a pre-selector for a radio receiver.
- 1 23. The integrated circuit of claim 19 further comprising:
2 a further bondwire connected between the die and a ground.
- 1 24. The integrated circuit of claim 19 further comprising:
2 a further bondwire connected between the die and a thermal pad.

1 25. An integrated circuit comprising:
2 a semiconductor die;
3 a first bondwire electrically connected to the die and a periphery pad;
4 a second bondwire electrically connected to the die and the periphery pad,
5 wherein:
6 the first and second bondwires are operable to act as an
7 autotransformer to form at least a part of a circuit block comprised within
8 the integrated circuit.

1 26. An integrated circuit comprising:
2 a semiconductor die;
3 a first bondwire electrically connected to the die and a first periphery pad;
4 a second bondwire electrically connected to the die and a second periphery
5 pad, wherein:
6 the first and second periphery pads are electrically connected, and
7 the first and second bondwires are operable to act as an
8 autotransformer to form at least a part of a circuit block comprised within
9 the integrated circuit.

1 27. An integrated circuit comprising:
2 a semiconductor die;
3 a first bondwire electrically connected to the die and a first periphery pad;
4 a second bondwire electrically connected to the die and a second periphery
5 pad, wherein:

the first and second bondwires are operable to act as a transformer to form at least a part of a circuit block comprised within the integrated circuit.

28. A method for creating a passive component within an integrated circuit comprising:

connecting a bondwire between a semiconductor die and a periphery pad wherein the bondwire is operable to act as an inductor forming at least a part of a circuit block comprised within the integrated circuit.

29. The method of claim 28 further comprising:

connecting a further bondwire between the semiconductor die and the periphery pad.

30. A method for creating a passive component within an integrated circuit comprising:

connecting a first bondwire between a semiconductor die and a first periphery pad;

connecting a second bondwire between a semiconductor die and a second periphery pad electrically connected to the first periphery pad;

wherein the bondwires are jointly operable to act as an autotransformer forming at least a part of a circuit block comprised within the integrated circuit.

31. A method for creating a passive component within an integrated circuit comprising:

connecting a first bondwire between a semiconductor die and a first periphery pad;

- 5 connecting a second bondwire between a semiconductor die and a second
6 periphery pad;
7 wherein the bondwires are jointly operable to act as a transformer forming
8 at least a part of a circuit block comprised within the integrated circuit

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